Claim Amendments

Claims 27 and 29 have been amended. Claims 17-21 and 28 have been canceled. Claims 1-16, 22-26 and 30-33 are unchanged. The following listing of claims replaces all previous versions of the claims in the application.

Listing of Claims

1. (original) An integrated circuit inductor formed in an interconnect dielectric stack on an integrated circuit, comprising:

at least two metal-layer conductive lines that run parallel to each other in respective metal-layer dielectric layers in the interconnect dielectric stack; and

at least one via-trench conductive line in a via-trench dielectric layer in the interconnect stack, wherein the via-trench conductive line lies between the two metal-layer conductive lines and electrically connects the two metal-layer conductive lines.

2. (original) The integrated circuit inductor defined in claim 1 wherein the metal-layer conductive lines and the via-trench conductive line comprise copper.

3. (original) The integrated circuit inductor defined in claim 1 wherein the metal-layer conductive lines each form a spiral between first and second inductor terminals.

4. (original) The integrated circuit inductor defined in claim 1 wherein there are at least three vertically-aligned metal-layer conductive lines that run parallel to each other, each in a different respective metal-layer dielectric layer in the interconnect dielectric stack, and wherein there are at least two sets of via-trench conductive lines, each set having at least one via-trench conductive line that electrically connects two of the three metal-layer conductive lines.

5. (original) The integrated circuit inductor defined in claim 1 comprising at least two via-trench conductive lines between the two metal-layer conductive lines, wherein the two via-trench conductive lines electrically connect the two metal-layer conductive lines.

6. (original) The integrated circuit inductor defined in claim 1 comprising at least two via-trench conductive lines between the two metal-layer conductive lines that electrically connect the two metal-layer conductive lines, wherein each via-trench conductive line has a bottom width and

an upper width and wherein the bottom widths are less than the upper widths so that the via trenches merge at the top of the via-trench conductive lines.

7. (original) The integrated circuit inductor defined in claim 1 wherein each of the metal-layer conductive lines has a length and the via-trench conductive line has a length, and wherein the length of the via-trench conductive line is equal to the length of the via-trench conductive lines.

8. (original) The integrated circuit inductor defined in claim 1 wherein the metal-layer conductive lines and the via-trench conductive line comprise copper and wherein the metal-layer conductive lines and via-trench conductive line are formed using a damascene semiconductor fabrication process.

9. (original) The integrated circuit inductor defined in claim 1 wherein the metal-layer conductive lines and the via-trench conductive line comprise copper and wherein at least one of the metal-layer conductive lines and the via-trench conductive lines are formed using a dual-damascene semiconductor fabrication process.

10. (original) The integrated circuit inductor defined in claim 1 wherein the interconnect dielectric stack has a top metal-layer dielectric layer, and wherein one of the metal-layer conductive lines is formed in the top metal-layer dielectric layer.

11. (original) The integrated circuit inductor defined in claim 1 wherein the metal-layer conductive lines comprise upper and lower parallel metal-layer conductive lines in the interconnect dielectric stack and wherein the lower parallel metal-layer conductive line has a concave upper surface due to dishing and the upper parallel metal-layer conductive line has a convex lower surface from being formed on top of the concave upper surface of the lower metal-layer conductive line.

12. (original) The integrated circuit inductor defined in claim 1 wherein the interconnect dielectric stack lies on the surface of a semiconductor substrate, the integrated circuit inductor further comprising a metal plate between the two metal layer conductive lines and the surface of the semiconductor substrate to reduce electromagnetic field interactions between the integrated circuit inductor and the semiconductor substrate.

13. (original) The integrated circuit inductor defined in claim 1 wherein the interconnect dielectric stack lies on the surface of a semiconductor substrate, the integrated circuit inductor further comprising a plurality of n-type and p-type wells at the surface of the semiconductor substrate that form a plurality of reverse-biased diodes that block eddy currents from flowing in the semiconductor substrate when the integrated circuit inductor is operated.

14. (original) The integrated circuit inductor defined in claim 13 wherein the n-type and p-type wells include at least some deep wells having depths greater than one micron.

15. (original) The integrated circuit inductor defined in claim 13 further comprising a region of shallow trench isolation that is formed on the surface of the semiconductor substrate between the n-type and p-type wells and the interconnect dielectric stack.

16. (original) The integrated circuit inductor defined in claim 13 wherein the two metal-layer conductive lines comprise at least two square metal-layer spirals interconnected by a square spiral via trench and wherein the square spirals have lateral dimensions of less than 200 microns.

17-21. (canceled)

22. (original) A method of forming an integrated circuit inductor for an integrated circuit with a dielectric interconnect stack on a semiconductor substrate, comprising:

forming at least two vertically-aligned metal-layer conductive lines in respective metal-layer dielectric layers in the dielectric interconnect stack using a damascene process; and

forming at least one via-trench conductive line in a via-layer dielectric layer in the dielectric interconnect stack using the damascene process, wherein the via-trench conductive line runs parallel to the two metal-layer conductive lines and electrically interconnects the two metal-layer conductive lines.

23. (original) The method defined in claim 22 wherein the integrated circuit inductor has a Q-factor, the method further comprising:

forming the conductive inductor line in a spiral; and

forming a region of n-type and p-type wells beneath the spiral to prevent eddy currents from reducing the Q-factor during operation of the inductor.

24. (original) The method defined in claim 22 further comprising forming a plurality of parallel via-trench conductive lines between the two metal-layer conductive lines.

25. (original) The method defined in claim 24 further comprising forming a plurality of parallel via-trench grooves for the parallel via-trench conductive lines using etching, wherein forming the parallel via-trench grooves comprises allowing the parallel via-trench grooves to merge during etching.

26. (original) The method defined in claim 22 further comprising using a copper dual-damascene fabrication process to form the metal-layer conductive lines and the via-trench conductive line.

27. (currently amended) An integrated circuit inductor formed in an interconnect dielectric stack on an integrated circuit, comprising:

at least three spiral metal-layer conductive lines that run parallel to each other in respective metal-layer dielectric layers in the interconnect dielectric stack; and

at least two ~~conductors~~ via-trench conductive lines each of which lies in a via-trench dielectric layer in the interconnect stack, wherein each ~~conductor~~ via-trench conductive line lies between a respective two of the metal-layer conductive lines and electrically connects those two metal-layer conductive lines.

28. (canceled)

29. (currently amended) The integrated circuit inductor defined in claim ~~28~~ 27 wherein the metal-layer conductive lines and the via-trench conductive lines comprise copper and wherein the metal-layer conductive lines and the via-trench conductive lines are formed using a dual-damascene semiconductor fabrication process.

30. (original) An integrated circuit inductor formed in an interconnect dielectric stack that lies on the surface of a semiconductor substrate in an integrated circuit, comprising:

at least two metal-layer conductive lines that run parallel to each other in respective metal-layer dielectric layers in the interconnect dielectric stack;

at least one conductor in a via-trench dielectric layer in the interconnect stack that electrically connects the two metal-layer conductive lines; and

a region of shallow trench isolation that is formed on the surface of the semiconductor substrate under the two metal-layer conductive lines.

31. (original) The integrated circuit inductor defined in claim 30 further comprising a plurality of n-type and p-type wells in the semiconductor substrate under the two metal-layer conductive lines that form a plurality of reverse-biased diodes that block eddy currents from flowing in the semiconductor substrate when the integrated circuit inductor is operated.

32. (original) The integrated circuit inductor defined in claim 31 wherein the conductor comprises a via-trench conductive line that runs parallel to the metal-layer conductive lines.

33. (original) The integrated circuit inductor defined in claim 32 wherein the two metal-layer conductive lines and the via-trench conductive line are spiral.